(12) UK Patent Application (19) GB (11) 2 358 737 (13) A

(43) Date of A Publication 01.08.2001

(21) Application No 0110041.1

(22) Date of Filing 01.03.2000

Date Lodged 24.04.2001

(30) Priority Data
(31) 11052323 (32) 01.03.1999 (33) JP

(62) Divided from Application No 0005006.2 under Section 15(4) of the Patents Act 1977

(71) Applicant(s)
NEC Corporation
(Incorporated in Japan)
7-1 Shiba 5-chome, Minato-ku, Tokyo 108-01, Japan

(72) Inventor(s)
Kiyoshi Takeuchi

(74) Agent and/or Address for Service
John Orchard & Co
Staple Inn Buildings North, High Holborn, LONDON,
WC1V 7PZ, United Kingdom

(51) INT CL[7]
H01L 27/092

(52) UK CL (Edition S)
H1K KGAFX K1CA K11B4 K11D K4C11 K4C14 K4H1A K4H3A K4H3X K9C2 K9D1 K9M1

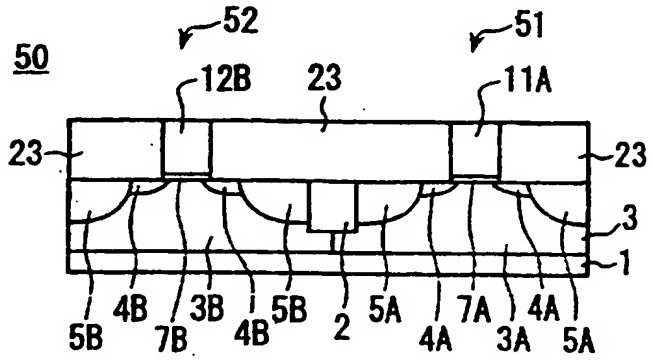
(56) Documents Cited
EP 0899784 A EP 0101960 A WO 00/19510 A

(58) Field of Search
UK CL (Edition S) H1K KCAL KGAFL KGAFX
INT CL[7] H01L 21/8238 27/092
EPOQUE: WPI, EPODOC, JAPIO

(54) Abstract Title
Methods for manufacturing a complimentary integrated circuit

(57) Two methods for manufacturing complimentary MOSFET devices are disclosed. The first (depicted in figs 1-3) comprises depositing dummy gate electrodes on a substrate, using these as ion implantation masks and then forming an insulation film over the substrate and dummy gate electrodes. The dummy electrodes are removed separately and the recesses left in the insulation film are individually filled with different gate electrode materials. The second method (depicted in figs 5 and 6) comprises separately forms gate electrodes of different material in recesses formde in an insulation layer and then uses these actual electrodes as implantation masks. Electrode materials, insulation layer materials and composite electrodes are all disclosed. The gate electrode materials preferably have a work function close to the work function of either n or p type polysilicon.

FIG. 4D



GB 2 358 737 A

FIG. 1A

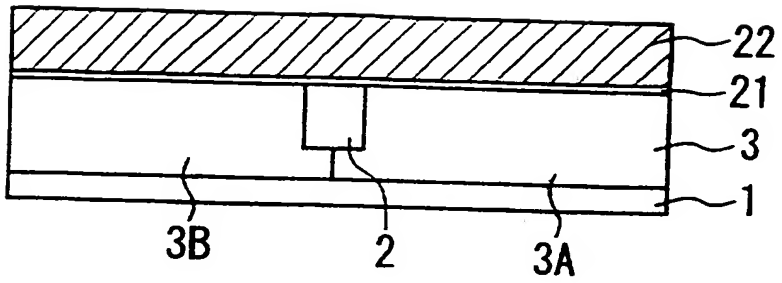


FIG. 1B

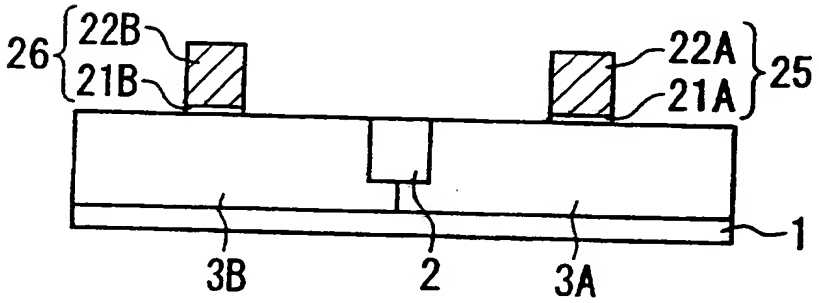


FIG. 1C

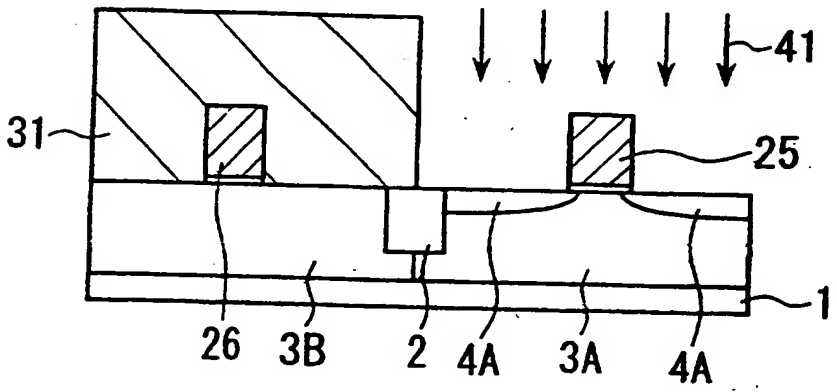


FIG. 1D

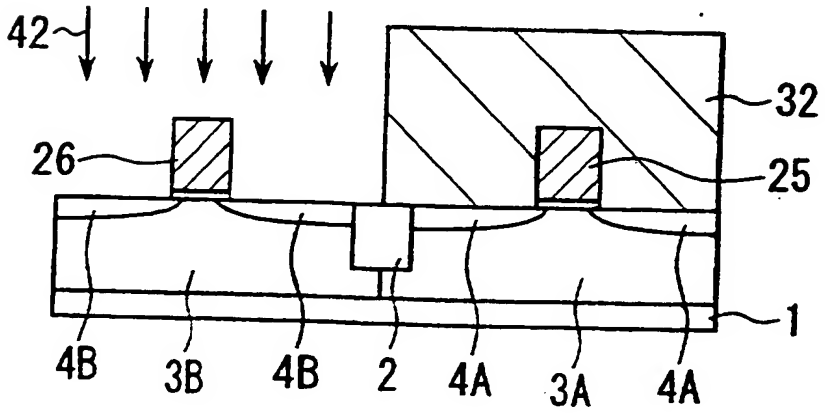


FIG. 2A

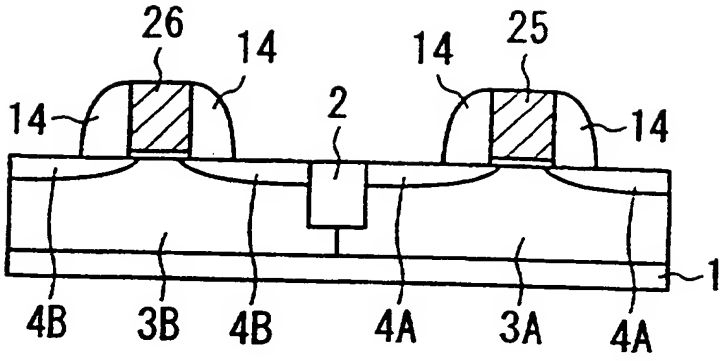


FIG. 2B

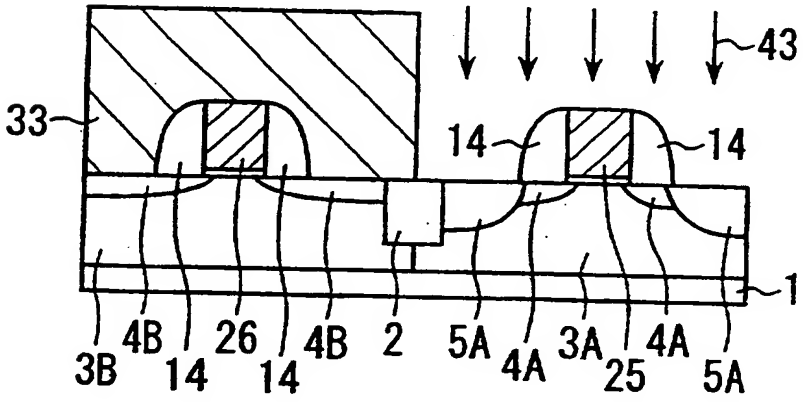


FIG. 2C

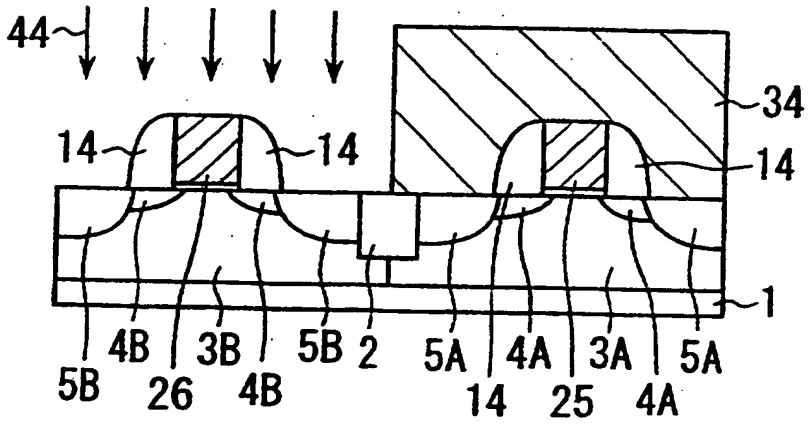


FIG. 2D

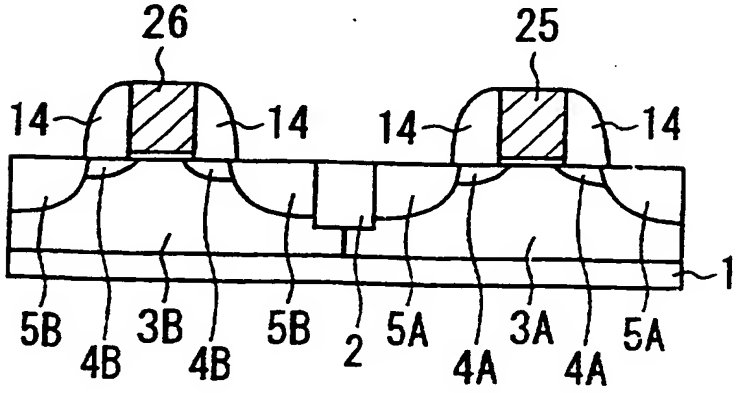


FIG. 3A

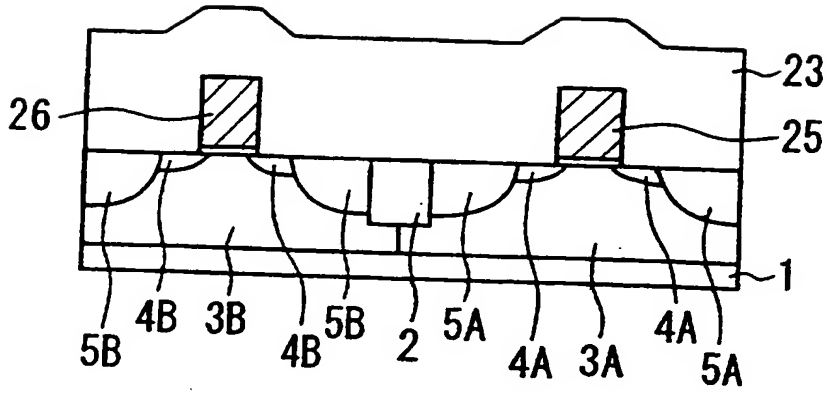


FIG. 3B

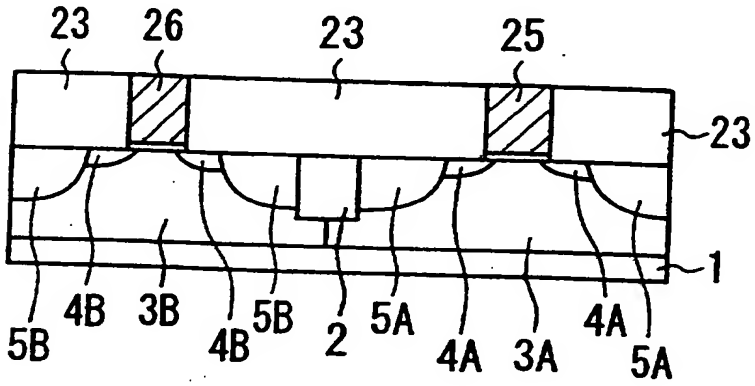


FIG. 3C

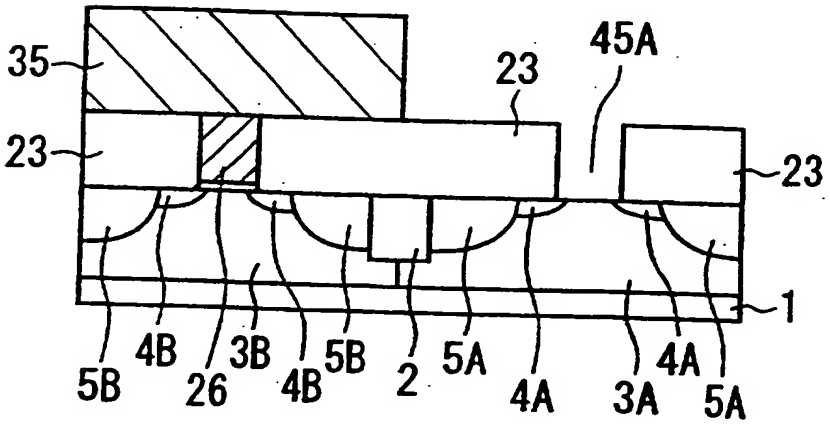


FIG. 3D

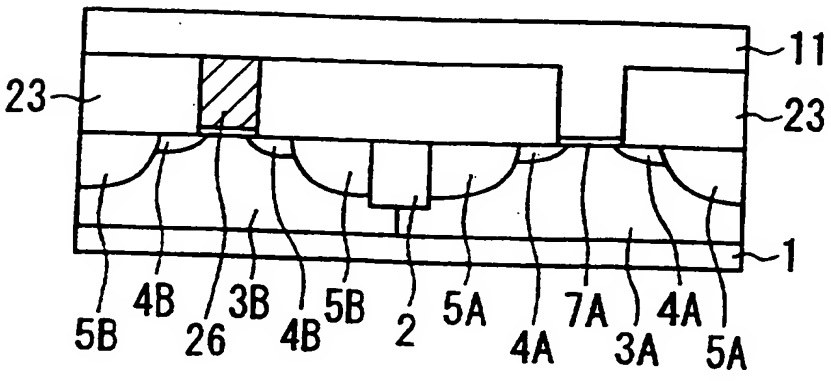


FIG. 4A

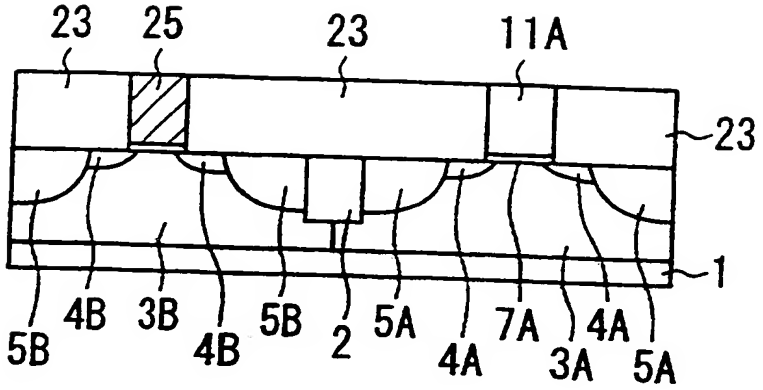


FIG. 4B

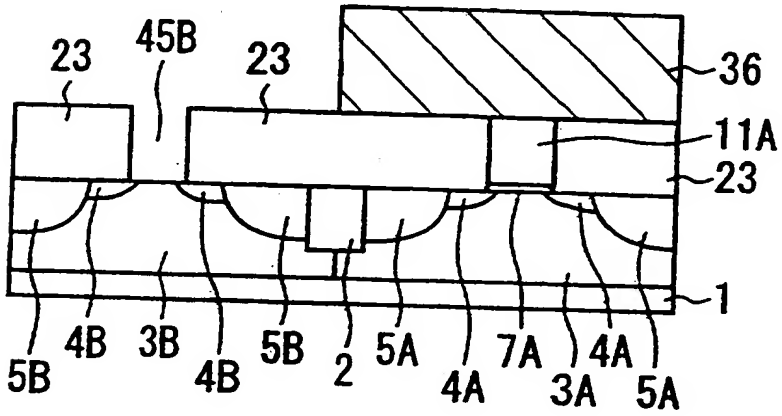


FIG. 4C

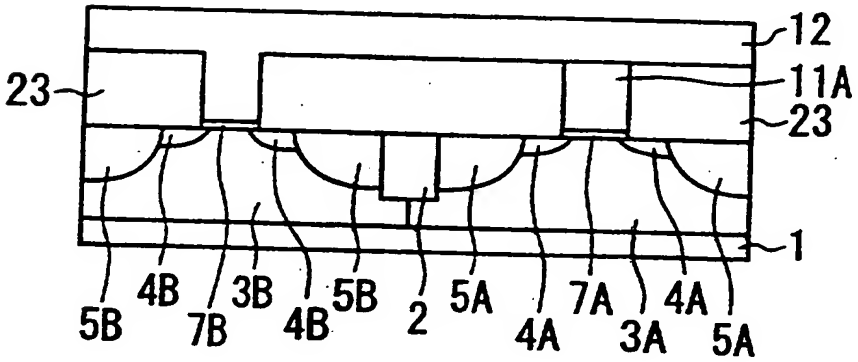


FIG. 4D

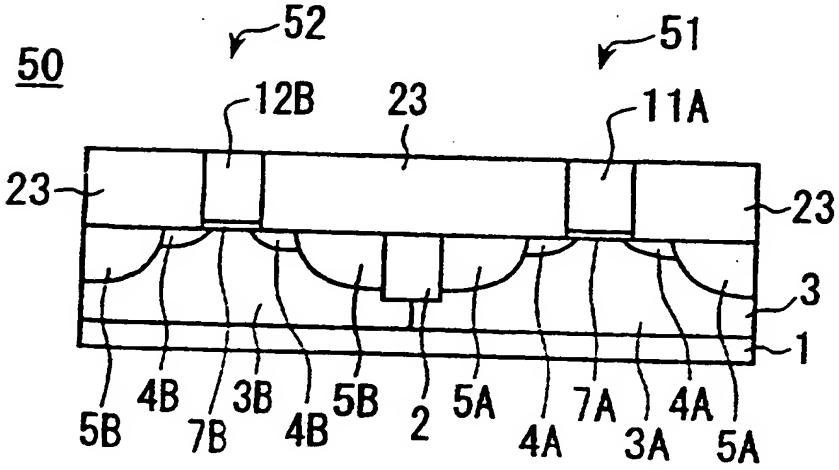


FIG. 5A

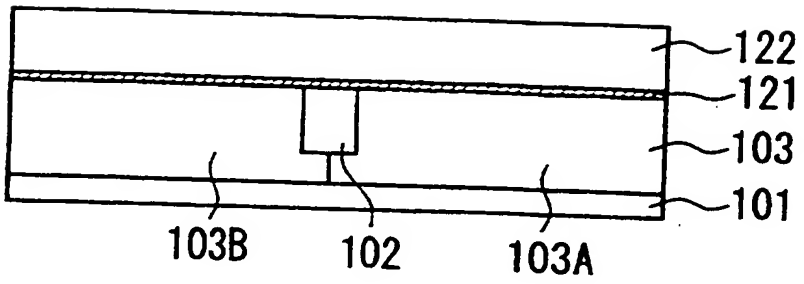


FIG. 5B

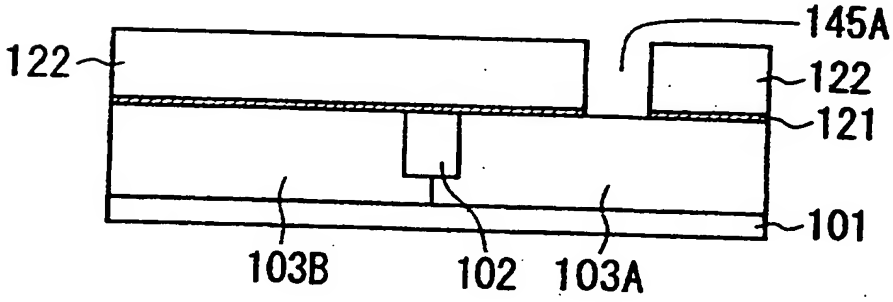


FIG. 5C

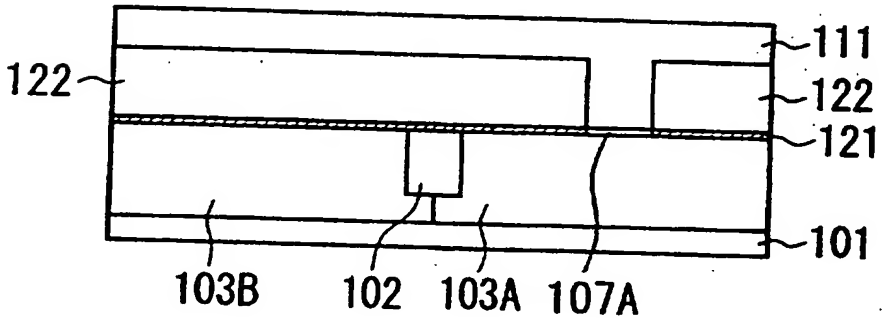


FIG. 5D

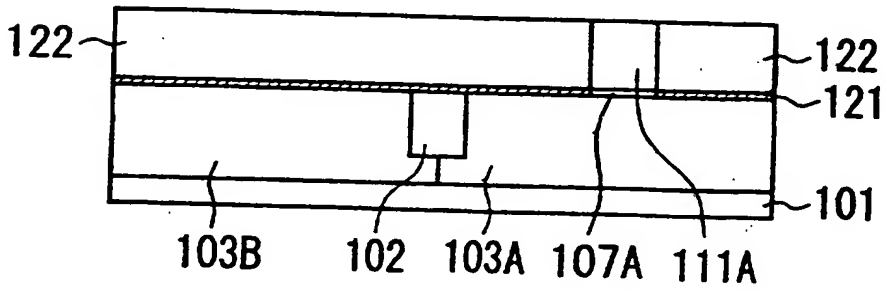


FIG. 5E

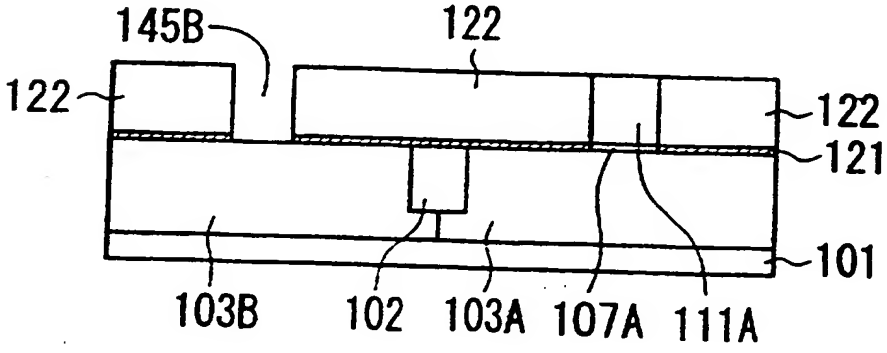


FIG. 6A

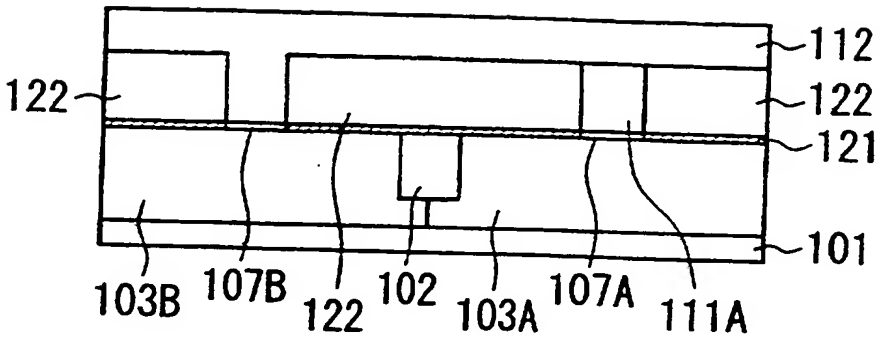


FIG. 6B

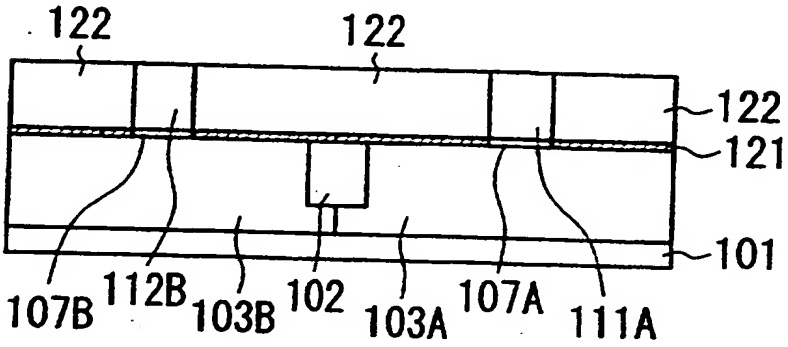


FIG. 6C

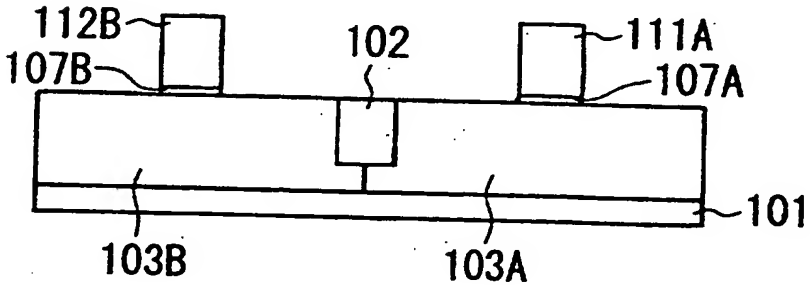


FIG. 6D

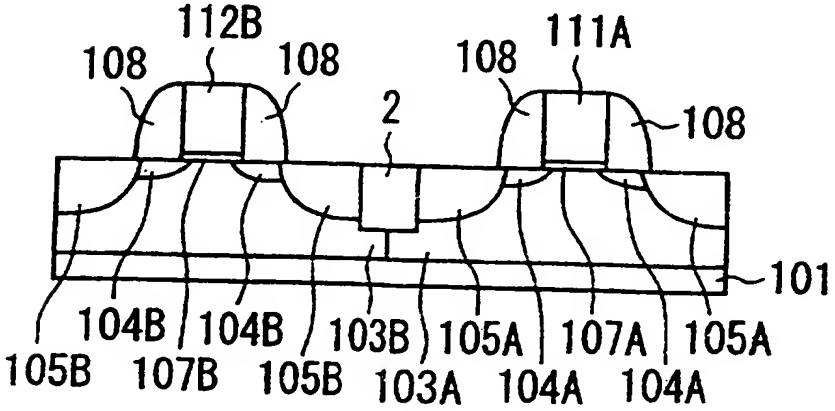


FIG. 7A

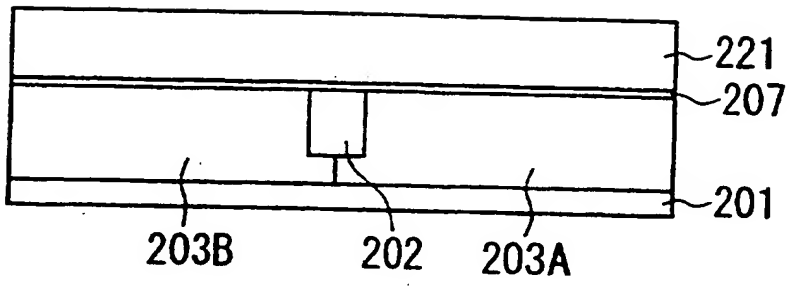


FIG. 7B

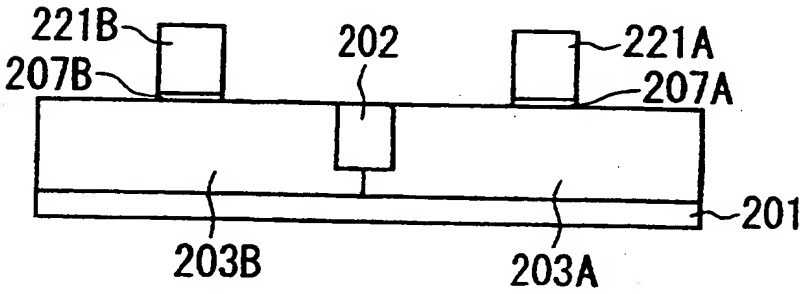


FIG. 7C

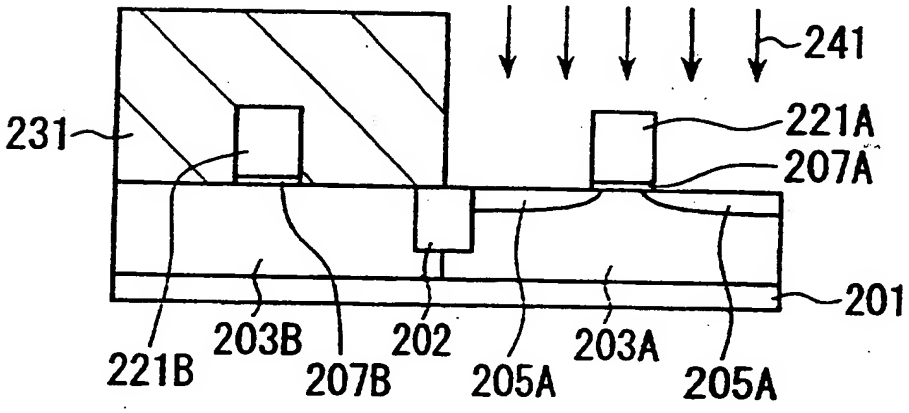
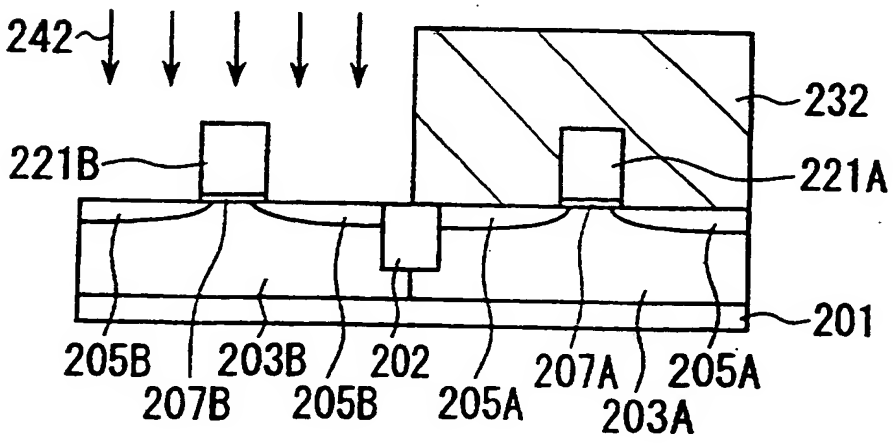


FIG. 7D



COMPLEMENTARY INTEGRATED CIRCUIT AND METHOD OF MANUFACTURE

The present invention relates generally to a complementary integrated circuit and a method of manufacturing the same. A particular arrangement relating to a complementary MISFET having a plurality of gate electrodes composed of different materials and its manufacturing method will be described below, by way of example in illustration of the present invention.

Complementary integrated circuits, especially complementary MISFET integrated circuits have previously been proposed. In such previously proposed complementary MISFET integrated circuits, for example, n-type polysilicon containing diffused phosphorus has been widely used as a material for gate electrodes.

The n-type polysilicon is advantageous in that it has a high resistance to heat and chemicals, that it is easy for a high-concentration impurity to be introduced, and that it is capable of providing a good interface with a gate insulating film, for example, it is capable of providing an interface having good adhesion to the gate insulating film. Use of the n-type polysiicon as the gate electrodes may however result in a p-channel FET having a higher threshold value than a desired value. A technique has thus been used for lowering the threshold value of the p-channel FET by means of counter doping. That is, a technique has been used in which, in the p-channel FET, the p-type impurity is introduced only in the vicinity of the surface of the substrate.

Nevertheless, with the miniaturization of the integrated circuits themselves, there has been a need to lessen the depth of the counter doping impurity to be introduced in the vicinity of the substrate surface,

making it difficult to implement a p-channel FET using the n-type polysilicon gate.

In order to deal with such a problem, in the case in which the gate length is, for example, 0.25 μ m or less, a so-called pn gate (or dual gate) configuration is employed in which the n-type polysilicon is used for the gate or gate electrode of the n- channel FET, and the p-type polysilicon is used for the gate or gate electrode of the p-channel FET.

Such a pn gate configuration makes use of gate materials suitable respectively for the n-channel type FET and the p-channel type FET, and it is possible to miniaturize the p-channel FET in particular, as compared with the conventional nn gate (or single gate) configuration which uses only the phosphorus diffused n-type polysilicon as a gate material of both the p-channel FET and the n-channel FET.

It is relatively easy in the pn gate configuration to provide two kinds of gate electrodes comprising mutually different gate materials on the same substrate. That is, polysilicon which does not contain impurity is first deposited on a substrate. Thereafter, n-type impurity is introduced only into an n-channel FET region and p-type impurity is introduced only into a p-channel FET region, locally by ion implantation. Thereby, an n-type polysilicon portion and a p-type polysilicon portion can be provideed on the substrate.

Reference will now be made to Figs. 7A - 7D of the accompanying drawings which show cross sectional views illustrating successive steps in a previously proposed method of manufacturing a complementary MISFET integrated circuit having a pn gate configuration.

First, as shown in FIG. 7A, a semiconductor layer is provided on an appropriate substrate 1, and an n-well region 203B and a p-well region 203A are provided via a predetermined element isolation region 202. Thereafter a gate insulating film 207 and a polysilicon film 221 are deposited thereon. Then, as shown in Fig. 7B, the polysilicon film 221 and the gate insulating film 207 are selectively removed by using a technique such as

photolithography and etching. Thereby, a gate electrode 221A is provided on a p-well region 203A via a gate insulating film 207A and a gate electrode 221B is provided on an n-well region 203B via a gate insulating film 207B.

Afterwards, as illustrated in FIG. 7C, for example, only a region corresponding to the p-channel FET is covered with a photo resist film 231 and an n-type impurity 241 is ion implanted only into a region corresponding to the n-channel FET. Thereby, the gate 221A of the n-channel FET is converted to an n-type gate, and n-type source/drain diffusion layers 205A are provided in the p-type well region 203A. Thereafter, the photo resist film 231 is removed. Subsequently, as shown in FIG. 7D, only a region corresponding to the n-channel FET is covered with a newly provided photo resist 232 and a p-type impurity 242 is ion implanted only into a region corresponding to the p-channel FET region. Thereby the gate 221B of the p-channel FET is converted to a p-type gate, and p-type source/drain diffusion layers 205B are provided in the n-type well region 203B. Thereafter, the photo resist film 232 is removed. Thus, the above-mentioned pn gate configuration is completed.

Furthermore, in a complementary MISFET integrated circuit including a combination of two different types of MISFETs, i.e., n-channel type and p-channel type MISFETs, it would be effective to provide respective gate electrodes by using different materials for the n-channel FETs and p-channel FETs, in order to achieve miniaturization or fining down and a high degree of integration of the MISFETs.

The reason is that the work functions, that is, electrical potentials peculiar to materials, of the gate materials suitable for obtaining good characteristics of FET's will be different in the n-channel FET and the p-channel FET, and hence that use of a single material as a gate material may make it difficult for the n-channel FET and the p-channel FET to offer good characteristics at the same time.

More specifically, when the gate material suitable for either one of the n-channel FET and the p-channel FET is used, a threshold value of the

other becomes higher than the desired value. In the event of a MISFET having a relatively large size, this deficiency could be overcome by controlling the threshold value by the counter doping method. With the progress of a MISFET toward miniaturization, it would however be necessary considerably to lessen the depth of and raise the concentration of the distribution of the impurity which is counter doped for controlling the threshold value. Therefore, it becomes difficult to apply the counter doping method thereto.

On the contrary, the pn gate configuration can be a technique for separately using two different gate materials for the n-channel FET and the p-channel FET. However, the conventional pn gate configuration may suffer from the problem that it is difficult sufficiently to increase the n-type or the p-type impurity concentration in the gate electrodes made of polysilicon.

More specifically, the impurity is introduced by ion implantation from the top surface of the gate electrode made of polysilicon, and thence moves by diffusion to the underside of the gate electrode made of polysilicon which is in contact with the gate insulating film. It would be limitative to raise the diffusion temperature or to extend the diffusion time, since it is necessary to avoid the occurrence of the phenomenon that the impurity, especially boron as a p-type impurity, penetrates through the gate insulating film.

Therefore, an impurity concentration in the vicinity of the underside of the gate electrode made of polysilicon becomes relatively low, so that, upon the operation of the FETs, a depletion layer may be provided in the vicinity of the underside of the gate electrode made of polysilicon. As a result thereof, the FET gate insulating film may have an increased effective thickness, leading to a deterioration in the performance of the FETs.

The influence of this gate depletion problem becomes more severe as the FETs get finer and as the gate insulating films get thinner, and it becomes remarkable, especially in case in which the gate length is approximately 0.1 μm or less.

On the other hand, it may be possible to solve the gate depletion

problem by using metals as the gate materials. The metals are not only free from the occurrence of the depletion, but they are also advantageous in that when metals are used as a gate material they often tend to lower the gate resistance.

It would also be effective to use, as the gate materials, semiconductors which are deposited while doping a high-concentration impurity. By doping the semiconductor during its deposition, impurity of a higher concentration can be introduced than by the ion implantation.

When the metallic materials or metal materials are used as the gate materials or the semiconductors, which are deposited while doping an impurity, are used as the gate materials, there arises the problem that it is difficult to provide two different types of gate electrodes composed of mutually different gate materials on the same substrate.

That is, it is impossible to use the method in which the gates are separately provided of two different gate materials by means of ion implantation, as in the conventional pn gate configuration.

In general, with respect to gate electrodes made of metallic materials, it is more difficult to carry out the the formation of gate electrodes by etching as compared with the case in which the gate electrodes are made of polysilicon.

Features of a complementary integrated circuit and a manufacturing method therefor to be described below, by way of example in illustration of the present invention are that gate electrodes are fabricated by using different gate materials for the n-channel FET and the p-channel FET, that the problem of gate depletion can be minimised, that a fine and high-performance complementary MISFET integrated circuit may be made comparatively easily, and that the difficulty in processing metallic materials and providing a complementary MISFET integrated circuit which uses different metallic gate materials for the n-channel FET and p-channel FET may be minimised.

In one arrangement to be described below, by way of example in

illustration of the present invention, an n-channel field effect transistor has a gate electrode in which at least a portion contacting a gate insulating film is made of a metal material having a work function close to the work function of n-type polysiicon.

In this case, it is preferable that the metal material consists of a material selected from a group consisting of zirconium and hafnium.

It is also preferable that at least a portion of the gate electrode in contact with a gate insulating film is made of the metal material, and a portion, other than the portion that is made of the metal material, is made of a material having a predetermined low electrical resistivity.

In another arrangement to be described below by way of example in illustration of the present invention, a p-channel field effect transistor has a gate electrode in which at least a portion contacting a gate insulating film is made of a metal material having a work function close to the work function of p-type polysilicon.

In this case, it is preferable that the metal material consists of a material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium rhenium and gold.

Rhenium is a particularly preferred metal material.

It is further preferable that at least a portion of the gate electrode in contact with a gate insulating film is made of the metal material, and a portion, other than the portion made of the metal material, is made of a material having a predetermined low electrical resistivity.

Another aspect of an arrangement to be described, by way of example in illustration of the present invention, is that a complementary integrated circuit includes an n-channel element having a gate electrode in which at least a portion contacting a gate insulating film is made of a first metal material having a work function close to the work function of n-type polysilicon; and a p-channel element having a gate electrode in which at least a portion contacting a gate insulating film is made of a second metal material having a work function close to the work function of p- type

polysilicon.

In this case, it is preferable that the first metal material is a material selected from a group consisting of zirconium and hafnium, and that the second metal material is a material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

A first metal material selected from a group consisting of zirconium and hafnium, and a second metal material of rhenium are particularly preferred.

It is further preferable that, in the gate electrode of the n-channel element, at least a portion of the gate electrode in contact with a gate insulating film is made of the first metal material, and that a portion, other than the portion made of the first metal material, is made of a material having a predetermined low electrical resistivity, that, in the gate electrode of the p-channel element, at least a portion of the gate electrode in contact with a gate insulating film is made of the second metal material, and that a portion, other than the portion made of the second metal material, is made of a material having a predetermined low electrical resistivity.

There will also be described, by way of example in illustration of the present invention a method of manufacturing a complementary integrated circuit, which includes the steps of preparing a semiconductor substrate, providing a region for providing an n-channel element and a region for providing a p-channel element on the semiconductor substrate via an element isolation region, providing a dummy gate electrode in each of the regions for providing an n-channel element and the region for providing a p-channel element, providing n-type diffusion regions in the region for providing an n-channel element and providing p-type diffusion regions in the region for providing a p-channel element; providing an insulating film over the entire surface of the semiconductor substrate, removing the dummy gate provided in one of the regions for providing an n-channel element and the region for providing a p-channel element to provide a first trench in the

insulating film; filling the first trench with a gate electrode material, removing the dummy gate provided in the other of the region for providing an n-channel element and the region for providing a p-channel element to provide a second trench in the insulating film, and filling the second trench with a gate electrode material.

In this case, it is preferable that, in the n-type diffusion regions provided in the region for providing an n-channel element and in the p-type diffusion regions provided in the region for providing a p-channel element, an n-type impurity is ion implanted into the regions for providing an n-channel element by using as a mask a resist film covering the region for providing a p-channel element and the dummy gate provided in the region for providing an n-channel element, and a p-type impurity is ion implanted into the region for providing a p-channel element by using as a mask a resist film covering the region for providing an n-channel element and the dummy gate provided in the region for providing the p-channel element.

It is also preferable that, in providing an insulating film over the entire surface of the semiconductor substrate, the insulating film is arranged so as to cover both the dummy gate provided in the region for providing an n-channel element and the dummy gate provided in the region for providing a p-channel element; and the method further includes, after the step of providing an insulating film over the entire surface of the semiconductor substrate, removing at least a portion of the insulating film to expose the upper surfaces of the dummy gate provided in the region for providing an n-channel element and the dummy gate provided in the region for providing a p-channel element.

It is further preferable that the method includes, after the step of removing the dummy gate provided in one of the regions for providing an n-channel element and in the region for providing a p-channel element to provide a first trench in the insulating film, providing a gate insulating film at the bottom portion of the first trench, wherein, in the step of filling the first trench with a gate electrode material, the first trench is filled with the gate

electrode material within the first trench and on the gate insulating film provided at the bottom portion of the first trench, wherein the method further includes, after the step of removing the dummy gate provided in the other of the regions for providing an n-channel element and in the region for providing a p-channel element a second trench is provided in the insulating film, providing a gate insulating film at the bottom portion of the second trench, and wherein, in the step of filling the second trench with the gate electrode material, the second trench is filled with the gate electrode material within the second trench and on the gate insulating film provided at the bottom portion of the second trench.

It is advantageous that, in the step of filling the first trench with a gate electrode material, a film made of the gate electrode material is provided on whole surface of the semiconductor substrate so as to fill the first trench and is polished to expose the upper surface of the insulating film, and wherein, in the step of filling the second trench with the gate electrode material, a film made of the gate electrode material is provided on the whole surface of the semiconductor substrate so as to fill the second trench and is polished to expose the upper surface of the insulating film.

It is also advantageous that a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes a metal material which has a work function close to the work function of n-type polysilicon at least at a bottom portion of the gate electrode material portion, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes a metal material which has a work function close to the work function of p-type polysiicon at least at a bottom portion of the gate electrode material portion.

It is further advantageous that a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes, at least at a bottom portion

thereof, a material selected from a group consisting of zirconium and hafnium, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

It is also preferable that a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, n-type polysiicon deposited while doping n-type impurity, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, p-type polysilicon deposited while doping p-type impurity.

It is further preferable that a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material having a work function close to the work function of n-type polysilicon and that the other portion of the gate electrode material portion includes a material having a predetermined low electrical resistivity, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material having a work function close to the work function of p-type polysilicon and that the other portion of the gate electrode material portion includes a material having a predetermined low electrical resistivity.

Yet another method of manufacturing a complementary integrated circuit to be described below, by way of example in illustration of the invention, includes the steps of preparing a semiconductor substrate, providing a region for providing an n-channel element and a region for providing a p-channel element on the semiconductor substrate via an

element isolation region, providing an insulating film over the entire surface of the semiconductor substrate, selectively removing the insulating film to provide a first trench in the insulating film on one of the regions for providing an n-channel element and the region for providing a p-channel element; filling the first trench with a gate electrode material, selectively removing the insulating film to provide a second trench in the insulating film on the other of the regions for providing an n-channel element and the region for providing a p-channel element, filling the second trench with a gate electrode material, removing the insulating film, providing n-type diffusion regions in the region for providing an n-channel element and providing p-type diffusion regions in the region for providing a p-channel element.

In this case, it is preferable that the method further includes, after the step of selectively removing the insulating film to provide a first trench in the insulating film on one of the regions for providing an n-channel element and the region for providing a p-channel element, providing a gate insulating film at the bottom portion of the first trench, wherein, in the step of filling the first trench with a gate electrode material, the first trench is filled with the gate electrode material within the first trench and on the gate insulating film provided at the bottom portion of the first trench, wherein the method further includes, after the step of selectively removing the insulating film to provide a second trench in the insulating film on the other of the regions for providing an n-channel element and on the region for providing a p-channel element, providing a gate insulating film at the bottom portion of the second trench, and wherein, in the step of filling the second trench with a gate electrode material, the second trench is filled with the gate electrode material within the second trench and on the gate insulating film provided at the bottom portion of the second trench.

It is also preferable that, in the step of filling the first trench with a gate electrode material, a film made of the gate electrode material is provided on whole surface of the semiconductor substrate, so as to fill the first trench, and is polished to expose the upper surface of the insulating

film, and wherein, in the step of filling the second trench with a gate electrode material, a film made of the gate electrode material is provided on the whole surface of the semiconductor substrate so as to fill the second trench and is polished to expose the upper surface of the insulating film.

It is further preferable that a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes a metal material which has a work function close to the work function of n-type polysilicon, at least at a bottom portion of the gate electrode material portion, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes a metal material which has a work function close to the work function of p-type polysilicon at least at a bottom portion of the gate electrode material portion.

It is advantageous that a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material selected from a group consisting of zirconium and hafnium, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

It is also advantageous that a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench comprises, at least at a bottom portion thereof, n-type polysilicon deposited while doping n-type impurity, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, p-type polysilicon deposited while doping p-type impurity.

It is further advantageous that a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material having a work function close to the work function of n-type polysiicon and the other portion of the gate electrode material portion includes a material having a predetermined low electrical resistivity, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material having a work function close to the work function of p-type polysilicon and the other portion of the gate electrode material portion includes a material having a predetermined low electrical resistivity.

In a complementary integrated circuit and in the method for its manufacture to be described below, by way of example in illustration of the present invention, it is possible to avoid the depletion of the gate, and also, by using gate materials having suitable work functions for the n-channel element and p-channel element respectively, it is possible to implement a fine and a high-performance complementary MISFET integrated circuit.

Furthermore, by using abrasive or etch back after filling the opening or trench with the electrode materials, in the provision of the electrodes, the second gate electrode can be processed and provided without affecting the previously provided first gate electrode. Therefore, it becomes possible readily to provide a plurality of different gate electrodes on the same substrate.

Furthermore, since the technique of separately providing the gates of different gate materials by ion implantation is not used, any materials may be selected as the gate materials.

Moreover, since etching is not used to process the gate electrodes, materials which are hard to etch may be applied to the gate electrodes, thereby providing a wider selection of the materials.

Arrangements illustrative of the invention will now be described, by

way of example with reference to the accompanying drawings, in which like reference numerals designate identical or corresponding parts and in which:

Figs. IA to 1D, Figs. 2A to 2D, Figs. 3A to 3D and Figs. 4A to 4D are schematic cross sectional views illustrating, in order of process steps, the structures of a complementary integrated circuit during manufacture, and

Figs. 5A to 5E and Figs. 6A to 6D are schematic cross sectional views illustrating, in order of process steps, the structures of another complementary integrated circuit during a manufacturing process.

Referring to the drawings and first to Fig. 4D, there is shown a complementary integrated circuit 50 which includes an n-channel element 51 having a gate electrode 11A made of a first metallic material or a metal material selected from a group consisting of zirconium and hafnium, and a p-channel element 52 having a gate electrode 12B made of a second metallic material or a metal material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

More specifically, the complementary integrated circuit 50 includes, as shown in Fig. 4D, a semiconductor layer 3 provided on an appropriate substrate 1, the semiconductor layer 3 including a p-well region 3A and an n-well region 3B which are provided via a predetermined element isolation region 2.

In the n-channel element 51, the gate electrode 11A of the first metallic material is provided on a part of the surface of the p-well region 3A via a gate insulating film 7A. Also, in the p-well region 3A and on both sides of the gate electrode 11A, diffusion layers 4A and 5A containing predetermined n-type impurities are provided. The diffusion layers 4A and 5A function as source/drain regions having an LDD structure.

Similarly, in the p-channel element 52 the gate electrode 12B of the second metal material is provided on part of the surface of the n-well region 3B via a gate insulating film 7B. Also, in the n-well region 3B and on both sides of the gate electrode 12B, diffusion layers 4B and 5B containing predetermined p-type impurities are provided. The diffusion layers 4B and

5B function as source/drain regions having an LDD structure. Also, the gate electrodes 11A and 12B are buried in an insulating film 23 if necessary. Although not shown in the drawing, it is possible to provide an interlayer insulating film on the insulating film 23 and the gate electrodes 11A and 12B, and, via through holes in the interlayer insulating film, to electrically couple the gate electrodes 11A and 12B and source/drain regions 5A and 5B with wiring, not shown in the drawing.

The second metal material is preferably rhenium.

In the arrangement being described, the semiconductor substrate could also be made of SOI (silicon on insulator) and in a such case the p-well region and the n-well region may not necessarily be provided separately especially for providing the n-channel element 51 and the p-channel element 52.

It is necessary in the present arrangement that the first metal material be one having a work function approximate to the work function of n^+ polysilicon and that the second metal material have a work function approximate to the work function of p^+ polysilicon.

As used herein, the work function refers to an electrical potential proper to that material.

Although in the above specific example, whole portions of the gate electrodes 11A and 12B are provided of the first and second metal materials, respectively, the scope of the protection sought is not limited to such configurations. For instance, the gate electrode 11A constituting the n-channel element 51 may employ a multi-layer structure consisting at least a lower layer made of the first metal material and being in contact with the gate insulating film 7A, and an upper layer made of a conductive material different from the first metal material and having a low electrical resistivity.

In the same manner, the gate electrode 12B making up the p-channel element 52 may employ a multi-layer structure including at least a lower layer made of the second metal material and being in contact with the gate insulating film 7B, and an upper layer made of a conductive material

different from the second metal material and having a low electrical resistivity.

Aluminium, tungsten, titanium, titanium nitride, etc., have hitherto been used as the metal gate materials although they were not the most suitable for both nMOSFETs and pMOSFETs, because their work functions are substantially intermediate between those of n^+ polysilicon and p^+ polysilicon.

It is considered that zirconium or hafnium are the optimum metal materials as the first metal material which has a work function closer to that of n^+ polysilicon that is most suitable for nMOSFETs.

In addition to their appropriate work functions, such metal materials have excellent features, such as a good chemical stability, a high anticorrosion factor as a result of the formation of a steady oxide layer in the air, and a high resistance to heat.

Since such materials have the disadvantage of high electrical resistivity, it is preferred that there be employed a two-layer or multi-layer gate electrode structure which includes a lower layer in contact with the gate insulating film and made mainly of the first metal material, and an upper layer made of a metal having a low resistivity. In this case, it is preferable that a film thickness of the first metal material, that is, zirconium or hafnium be approximately 3 nm or more.

The metal providing the upper layer in the gate electrode 11A is preferably tungsten having a low electrical resistivity and being easy to process. Also, depending on the situation, various metal silicides, such as titanium silicide and the like which are widely used in the conventional silicon processes, may be used.

Furthermore, between the lower layer portion made of the first metal material and the upper layer portion made of tungsten and the like, there is preferably provided an adhesion layer of titanium nitride, tungsten nitride or the like.

It has further been found that platinum silicide, iridium silicide, cobalt,

nickel, rhodium, palladium, rhenium, gold, etc. are most suitable as the second metal material having a work function closer to that of p^+ polysilicon which is the optimum material for pMOSFETs. In the present arrangement, one metal material selected from the group of metal materials is used as a material of the gate electrode 12B of the p-channel element 52.

Similar to nMOSFETs, in respect of such metals as well, the gate electrode is preferably of the two-layer or multi-layer structure in which the second metal material is used for the lower layer portion of the gate electrode 12B in contact with the gate insulating film 7B and a metal having low electrical resistivity is used for the upper layer portion thereof.

The present arrangement is effective even in cases in which n^+ polysilicon is used for the gate electrodes of nMOSFETs or where p^+ polysilicon is used for the gate electrodes of pMOSFETs.

More specifically, the use of the manufacturing method to be described herein, by way of example, will allow the gate materials of the nMOSFETs and pMOSFETs to be separately deposited, so that it is possible to introduce n-type or p-type impurities with a high concentration into polysiicon simultaneously with the deposition, in place of introducing impurities into the polysiicon by ion implantation. This process is carried out, for example, by depositing polysilicon while doping an impurity by using doping gas, when polysilicn is deposited by a CVD method.

By using such a method, it is possible to raise the impurity concentration in the vicinity of the gate insulating film in a gate electrode made of polysilicon, as compared with a previously proposed method, thereby making it possible to restrain the gate depletion.

In such case, the multi-layer structure could be employed in order to diminish the resistance of the gate electrode, with the use of n^+ polysilicon or p^+ polysiicon only in the lower layer portions in contact with the gate insulating film, and with the use of a conductive material having low electrical resistivity in the upper layer portions of gate electrodes.

A detailed description will now be made of a specific example of a

complementary integrated circuit and of its method of manufacture, with reference to the drawings.

Figs. 1A to 1D, Figs. 2A to 2D, Figs. 3A to 3D and Figs. 4A to 4D, show cross sections of the complementary MISFET integrated circuit 50 during manufacture.

In this specific example, the source/drain diffusion layers are provided previous to the formation of the gate electrodes.

First, as shown in Fig. 1A, the p-well 3A, the n-well 5B and the element isolation insulating film 2 are provided either on a semiconductor layer 3 on the semiconductor substrate 1, or on the semiconductor substrate 1 itself, after which a protection film 21 and a film 22 are deposited in sequence.

As shown in Fig. 1B, using ordinary photolithography and etching, the protection film 21. and the film 22 are selectively removed, and dummy gates 25 and 26 are provided by leaving portions 21A and 21B of the protection film 21 and portions 22A and 22B of the film 22 only at regions at which the gate electrodes are to be provided.

Next, as shown in Fig. 1C, only the p-channel element region is then covered with a photo resist film 31, and n-type impurities 41 are ion implanted into the n-channel element region by using the dummy gate 25 as a mask to provide a shallow n-type source/drain diffusion layer 4A in the p-well 3A.

As shown in Fig. 1D, the photo resist film 31 is then stripped off and only the n-channel element region is newly covered with a photo resist film 32, and the p-type impurities 42 are ion implanted into the p-channel element region by using the dummy gate 26 as a mask to provide a shallow p-type source/drain diffusion layer 4B in the n-well 3B.

As shown in Fig. 2A, the photo resist film 32 is then stripped off, and side wall insulating film spacers 14 composed of silicon oxide films and the like are provided at the sides of the dummy gates 25 and 26 by an ordinary technique using CVD and etch back.

Next, as shown in Fig. 2B, only the p-channel element region is then covered with a photo resist film 33, and n-type impurities 43 are ion implanted into the n-channel element region by using the dummy gate 25 and the side wall insulating film spacers 14 as a mask to provide a deep p-type source/drain diffusion layer 5A in the p-well 3A.

As shown in Fig. 2C, the photo resist film 33 is then stripped off and only the n-channel element region is newly covered with a photo resist film 34, and the p-type impurities 44 are ion implanted into the p-channel element region by using the dummy gate 26 and side wall insulating film spacers 14 as a mask to provide a deep p-type source/drain diffusion layer 5B in the n-well 3B.

It is also possible to make an impurity concentration of the source/drain diffusion layers 5A and 5B larger than that of the source/drain diffusion layers 4A and 4B. Then, as shown in Fig. 2D, the resist film 34 is removed.

As shown in Fig. 3A, an insulating film 23, which may be made of silicon oxide and the like is then deposited on the overall surface of the substrate. In this arrangement, since the sidewall insulating film spacers 14 and the insulating film 23 are both provided of silicon oxide films, interface portions therebetween are not illustrated in the drawings after Fig. 3A. Then, as shown in Fig. 3B, the upper surface of the insulating film 23 is planarized by ordinary abrasion, polishing or etch back so as to allow the top of the dummy gates 25 and 26 to be exposed.

As shown in Fig. 3C, only the p-channel element region is then covered with a photo resist film 35, and only the dummy gate 25 in the n-channel element region is selectively removed. Thereby, an opening or trench 45A is provided in the insulating film 23.

As shown in Fig. 3D, the photo resist film 35 is then stripped off, and, by the oxidation of the substrate or by the deposition of an insulating film, a gate insulating film 7A is provided at the bottom portion of the trench 45A. A gate electrode material film 11 for an n-channel FET made of the

above-mentioned first metal material is further deposited on whole area of the substrate so as to fill up the trench 45A.

As shown in Fig. 4A, the gate electrode material film 11 is then abraded, polished or etched back until the surface of the insulating film 23 is exposed. Thereby, the gate electrode 11A for an n-channel FET is provided.

As shown in Fig. 4B, only the n-channel element region is then covered with a photo resist film 36, and only the dummy gate 26 in the p-channel element region is selectively removed. Thereby, an opening or trench 45B is provided in the insulating film 23.

As shown in Fig. 4C, the photo resist film 36 is then stripped off, and, by the oxidation of the substrate or by the deposition of an insulating film, a gate insulating film 7B is provided at the bottom portion of the trench 45B. A gate electrode material film 12 for a p-channel FET made of the above-mentioned second metal material is further deposited on whole area of the substrate so as to fill up the trench 45B.

As shown in Fig. 4D, the gate electrode material film 12 is then abraded or etched back until the surface of the insulating film 23 is exposed. Thereby, the gate electrode 12B for a p-channel FET is provided.

Thereby, the structure of Fig. 4D is completed. The MISFET 50 is thereafter completed as a complementary integrated circuit through deposition of interlayer insulating films, the formation of connection openings reaching the source/drain diffusion layers and the gate electrodes in the interlayer insulating film, and the formation of wiring.

In such a specific example, a silicon oxide film, a polysilicon and a silicon oxide film can be utilized in combination, as the protection film 21, the film 22 and the insulating film 23, respectively. By using such layered films, it is possible, in the process of removing the dummy gates 25 and 26 in Fig. 3C and Fig. 4B, first to remove selectively only the polysilicon 22A or 22B through etching which uses chlorine gas, for example, and then to remove the thin silicon oxide film 21A or 21B by means of less damaging etching which uses HF (hydrogen fluoride), for example.

The bottom portions of the trenches 45A and 45B must be subjected to even less damage since they provide channels of the FETs. Provision of the protection film 21, that is, 21A and 21B, will fulfill such a requirement.

With reference to Figs. 5A to 5E and Figs. 6A to 6D, a detailed description will now be given of the configuration of another specific example of a complementary integrated circuit and the method of its manufacture.

That is, referring to Figs. 5A to 5E and Figs. 6A to 6D, there are shown cross sections of a complementary MISFET integrated circuit during manufacture.

In this specific example the source/drain diffusion layers are provided after the formation of the gate electrodes.

First, as shown in Fig. 5A, a p-well 103A, an n-well 103B and an element isolation insulating film 102 are formed on a semiconductor layer 103 provided on a semiconductor substrate 101, or on the semiconductor substrate 101 itself in a known manner, after which a protection film 121 and a film 122 are deposited in sequence.

The protection film 121 and the film 122 can be, for example, a silicon nitride film and a silicon oxide film, respectively.

As shown in Fig. 5B, using ordinary photolithography and etching, the protection film 121 and the film 122 are then selectively removed, and an opening or trench 145A is provided at the location at which the gate electrode of an n-channel FET is to be provided.

Then, as shown in Fig. 5C, a gate insulating film 107A is provided at the bottom portion of the trench 145A by the oxidation of the substrate or by deposition of an insulating film, and a film 111 including the above-mentioned first metal material for a gate electrode of an n-channel FET is deposited thereon so as to fill up the trench 145A.

As shown in Fig. 5D, the film 111 for a gate electrode is then abraded or etched back until the surface of the insulating film 122 becomes exposed. Thereby, the gate electrode 111A for an n-channel FET is completed.

As shown in Fig. 5E, using ordinary photolithography and etching, the protection film 121 and the film 122 are then selectively removed, and an opening or trench 145B is provided at the location at which the gate electrode of a p-channel FET is to be provided.

Then, as shown in Fig. 6A, a gate insulating film 107B is formed at the bottom portion of the trench 145B by the oxidation of the substrate, or by the deposition of an insulating film, and a film 112 including the above-mentioned second metal material for a gate electrode of a p-channel FET is deposited thereon so as to fill up the trench 145B.

As shown in Fig. 6B, the film 112 for a gate electrode is then abraded or etched back until the surface of the insulating film 122 becomes exposed. Thereby, the gate electrode 112B for a p-channel FET is completed.

As shown in Fig. 6C, the remaining films 121 and 122 are then selectively removed by etching.

In the case in which the film 122 is a silicon oxide film, hydrogen fluoride can be used for etching. It is to be noted that if the film 121 is thin, it may remain undisturbed. Afterwards, sidewall insulating film spacers 108 are provided, and, by ion implantation and the like, source/drain diffusion layers 4A, 5A, 4B and 5B are provided. These process steps are substantially the same as those mentioned with reference to Fig. 1C to Fig. 2D, and a detailed description thereof is omitted here. Thereby, a structure as shown in Fig. 6D is obtained.

The MISFET which is a complementary integrated circuit is thereafter completed through the deposition of interlayer insulating films, the formation of connection openings reaching the source/drain diffusion layers and the gate electrodes in the interlayer insulating film, and the formation of wiring.

In the manufacturing process of the above-mentioned embodiment, the gate electrode 11A or 111A remains buried in the insulating film 23 or 122 during the the formation of the subsequently provided gate electrode

12B or 112B. For this reason, the step of providing the gate electrode 12B or 112B will not interfere with the gate electrode 11A or 111A, thus advantageously enabling the two different kinds of gate electrode to readily and separately be provided on the same substrate.

Furthermore, the processing of the gate material films 11 and 12, or 111 and 112 to provide the gate electrodes can be effected by abrasion or polishing, for example, chemical mechanical polishing (CMP), mechanical polishing and the like. For this reason, it will be possible even for the materials which are hard to etch to be processed, thus conveniently providing more choice in the materials used for providing the gate electrodes.

The above embodiment is arranged such that the source/drain diffusion layers 4A and 5A are self-aligned with the gate electrode 11A and that the source/drain diffusion layers 4B and 5B are self-aligned with the gate electrode 12B. Similarly, the source/drain diffusion layers 104A and 105A are self-aligned with the gate electrode 111A and the source/drain diffusion layers 104B and l05B are self-aligned with the gate electrode 112B. Therefore, the present arrangement is applicable to any fine MISFETs of 0.1 μm or less.

Usable as the gate electrode material film 11 or 111 for an n-channel element is a stable metal such as zirconium or hafnium having an appropriate work function. Alternatively, it is possible to use highly doped n-type polysilicon which is deposited while doping with, e.g., phosphorus or polysilicon doped with, e.g., phosphorus by diffusion from a gas source as the gate electrode material film 11 or 111 for an n-channel element. Available as the gate electrode material film 12 or 112 for a p-channel element is a stable metal, e.g., rhenium having an appropriate work function. Alternatively, it is possible to use highly doped p-type polysilicon which is deposited while doping with boron. In either case, the gate is restrained from becoming depleted as compared with the previously proposed pn gate configuration, where the gate electrodes are doped by using ion

implantation.

The above description has been made with an illustration of the case in which the gate electrodes are of a single layer. However, the gate electrodes may be provided of a plurality of layered materials for the purpose of, e.g., reducing the resistance. For example, the lower and upper layers can be made respectively of a material for determining the work function and a material having a low resistance. To this end, the gate electrode material films 11 and 12 of Fig. 3D and Fig. 4C, or the gate electrode material films 111 and 112 of Fig. 5C and Fig. 6A may provide the laminated films, or multi-layered films.

In such a case, the gate electrode materials of the above description refer to materials at the lowest ends of the gate electrodes, that is, materials at portions in contact with the gate insulating films. This is due to the fact that the work function to determine the characteristics of the FETs is determined by the lowermost layer of the gate electrodes. When the gate electrodes are made of the lamination of a plurality of film materials, the n-channel FET and the p-channel FET can include the same gate electrode layers except the lowest ends thereof.

In the above case, the FETs have had the source/drain diffusion layers each consisting of a shallow portion and a deep portion. However, the source/drain diffusion layers can be of a so-called single drain structure having a single depth. In such a case, the steps corresponding to Fig. 2A to Fig. 2D can be eliminated.

As has been explained above, the present arrangement enables a complementary MISFET integrated circuit to be made which is easy to manufacture and capable of achieving both miniaturization and enhancement of performance, compared with basic configurations. Thus ensuring that miniaturization is facilitated by allowing the use of different gate electrode materials for the n-channel element and the p-channel element, that high performances is achieved by restraining the gates from becoming depleted, and that the configuration, which includes a plurality of gate materials can

easily be manufactured by employing a manufacturing method in which the gates are buried in the trenches.

It will be understood that, although particular arrangements illustrative of the invention have been described, by way of example, variations and modifications thereof, as well as other arrangements may be conceived within the scope of the appended claims.

CLAIMS

1. A method of manufacturing a complementary integrated circuit, including preparing a semiconductor substrate, providing a region for providing an n-channel element and a region for providing a p-channel element on the semiconductor substrate via an element isolation region; providing a dummy gate electrode in each of the regions for providing an n-channel element and in the region for providing a p-channel element; providing n-type diffusion regions in the region for providing an n-channel element and providing p-type diffusion regions in the region for providing a p-channel element; providing an insulating film over the entire surface of the semiconductor substrate, removing the dummy gate provided in one of the regions for providing an n-channel element and in the region for providing a p-channel element to provide a first trench in the insulating film; filling the first trench with a gate electrode material, removing the dummy gate provided in the other of the regions for providing an n-channel element and in the region for providing a p-channel element to provide a second trench in the insulating film, and filling the second trench with a gate electrode material.

2. A method of manufacturing a complementary integrated circuit as claimed in claim 1, wherein, in the step of providing n-type diffusion regions in the region for providing an n-channel element, and providing p-type diffusion regions in the region for providing a p-channel element, an n-type impurity is ion implanted into the region for providing an n-channel element by using, as a mask, a resist film covering the region for providing a p-channel element and the dummy gate provided in the region for providing an n-channel element, and a p-type impurity is ion implanted into the region for providing a p-channel element by using, as a mask, a resist film covering the region for providing an n-channel element and the dummy gate provided in the region for providing a p-channel element.

3. A method of manufacturing a complementary integrated circuit as claimed in claim 1, wherein, in the step of providing an insulating film over the entire surface of the semiconductor substrate, the insulating film is provided so as to cover the dummy gate provided in the region for providing an n-channel element and the dummy gate provided in the region for providing a p-channel element, in which the method further includes, after the step of providing an insulating film over the entire surface of the semiconductor substrate, removing at least a portion of the insulating film to expose the upper surfaces of the dummy gate provided in the region for providing an n-channel element, and the dummy gate provided in the region for providing a p-channel element.

4. A method of manufacturing a complementary integrated circuit as claimed in claim 1, wherein the method further includes, after the step of removing the dummy gate provided in one of the region for providing an n-channel element and the regions for providing a p-channel element, providing a first trench in the insulating film, providing a gate insulating film at the bottom portion of the first trench, wherein, in the step of filling the first trench with a gate electrode material, the first trench is filled with the gate electrode material within the first trench and on the gate insulating film provided at the bottom portion of the first trench, wherein the method further includes, after the step of removing the dummy gate provided in the other of the regions for providing an n-channel element and in the region for providing a p-channel element, the steps of providing a second trench in the insulating film, and providing a gate insulating film at the bottom portion of the second trench, and wherein, in the step of filling the second trench with the gate electrode material, the second trench is filled with the gate electrode material within the second trench and on the gate insulating film provided at the bottom portion of the second trench.

5. A method of manufacturing a complementary integrated circuit as claimed in claim 1, wherein, in the step of filling the first trench with a gate

electrode material, a film made of the gate electrode material is provided on whole surface of the semiconductor substrate so as to fill the first trench and is polished to expose the upper surface of the insulating film, and wherein, in the step of filling the second trench with the gate electrode material, a film made of the gate electrode material is provided on whole surface of the semiconductor substrate so as to fill the second trench and is polished to expose the upper surface of the insulating film.

6. A method of manufacturing a complementary integrated circuit as claimed in claim 1, wherein a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes a metal material which has a work function close to the work function of n-type polysilicon at least at a bottom portion of the gate electrode material portion, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes a metal material which has a work function close to the work function of p-type polysilicon at least at a bottom portion of the gate electrode material portion.

7. A method of manufacturing a complementary integrated circuit as claimed in claim 1, wherein a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material selected from a group consisting of zirconium and hafnium, and wherein a gate electrode material portion filling a trench provided in the region for providing an p-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

8. A method of manufacturing a complementary integrated circuit as claimed in claim 1, wherein a gate electrode material portion filling a trench

provided in the region for providing an n-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, n-type polysilicon deposited while doping n-type impurity, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, p-type polysilicon deposited while doping p-type impurity

9. A method of manufacturing a complementary integrated circuit as claimed in claim 1, wherein a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material having a work function close to the work function of n-type polysilicon and the other portion of the gate electrode material portion includes a material having a predetermined low electrical resistivity, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material having a work function close to the work function of p-type polysilicon and the other portion of the gate electrode material portion includes a material having a predetermined low electrical resistivity.

10. A method of manufacturing a complementary integrated circuit, including preparing a semiconductor substrate; providing a region for providing an n-channel element and a region for providing a p-channel element on the semiconductor substrate via an element isolation region; providing an insulating film over the entire surface of the semiconductor substrate; selectively removing the insulating film to provide a first trench in the insulating film on one of the regions for providing an n-channel element and the region for providing a p-channel element; filling the first trench with a gate electrode material; selectively removing the insulating film to provide a second trench in the insulating film on the other of the regions for providing

an n-channel element and on the region for providing a p-channel element; filling the second trench with a gate electrode material; removing the insulating film; providing n-type diffusion regions in the region for providing an n-channel element and providing p-type diffusion regions in the region for providing a p-channel element.

11. A method of manufacturing a complementary integrated circuit as claimed in claim 10, wherein the method further includes, after the step of selectively removing the insulating film to provide a first trench in the insulating film on one of the regions for providing an n-channel element and the region for providing a p-channel element, providing a gate insulating film at the bottom portion of the first trench, wherein, in the step of filling the first trench with a gate electrode material, the first trench is filled with the gate electrode material within the first trench and on the gate insulating film provided at the bottom portion of the first trench, wherein the method further includes, after the step of selectively removing the insulating film to provide a second trench in the insulating film on the other of the region for providing an n-channel element and the regions for providing a p-channel element, providing a gate insulating film at the bottom portion of the second trench, and wherein, in the step of filling the second trench with a gate electrode material, the second trench is filled with the gate electrode material within the second trench and on the gate insulating film provided at the bottom portion of the second trench.

12. A method of manufacturing a complementary integrated circuit as claimed in claim 10, wherein, in the step of filling the first trench with a gate electrode material, a film made of the gate electrode material is provided on whole surface of the semiconductor substrate so as to fill the first trench and is polished to expose the upper surface of the insulating film, and wherein, in the step of filling the second trench with a gate electrode material, a film made of the gate electrode material is provided on whole surface of the semiconductor substrate so as to fill the second trench and is polished to

expose the upper surface of the insulating film.

13. A method of manufacturing a complementary integrated circuit as claimed in claim 10, wherein a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes a metal material which has a work function close to the work function of n-type polysilicon at least at a bottom portion of the gate electrode material portion, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes a metal material which has a work function close to the work function of p-type polysilicon at least at a bottom portion of the gate electrode material portion.

14. A method of manufacturing a complementary integrated circuit as claimed in claim 10, wherein a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material selected from a group consisting of zirconium and hafnium, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material selected from a group consisting of platinum silicide, iridium silicide, cobalt, nickel, rhodium, palladium, rhenium and gold.

15. A method of manufacturing a complementary integrated circuit as claimed in claim 10, wherein a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, n-type polysilicon deposited while doping n-type impurity, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, p-type polysilicon deposited while doping

p-type impurity.

16. A method of manufacturing a complementary integrated circuit as claimed in claim 10, wherein a gate electrode material portion filling a trench provided in the region for providing an n-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material having a work function close to the work function of n-type polysilicon and other portion of the gate electrode material portion includes a material having a predetermined low electrical resistivity, and wherein a gate electrode material portion filling a trench provided in the region for providing a p-channel element among the first trench and the second trench includes, at least at a bottom portion thereof, a material having a work function close to the work function of p-type polysilicon and the other portion of the gate electrode material portion includes a material having a predetermined low electrical resistivity.

17. A method of manufacturing a complementary integrated circuit as claimed in claim 1 substantially as described herein with reference to Figs. 1 to 6 of the accompanying drawings.

18. A complementary integrated circuit made by a method as claimed in any one of the preceding claims.